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10/690,006	10/21/2003	Robert M. Steinhoff	TI-35703	4784

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EXAMINER	
ARENA, ANDREW OWENS	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 09/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/690,006	STEINHOFF ET AL.	
	Examiner	Art Unit	
	Andrew O. Arena	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/21/03, 11/17/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "n-moat-p-well diode" of line 2 of claim 6 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: ESD protection for integrated circuits provided by series connected bipolar transistors sharing common collector region.

Claim Objections

3. Claim 18 is objected to because of the following informalities: lines 4-5 are repeated in lines 6-8. Since the limitations of lines 4-5 are included in lines 6-8, lines 4-5 should be eliminated.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 2, 7-16, and 18-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Clukey (US 5,644,460), hereinafter Clukey.

6. Regarding claim 1, Clukey discloses (Fig 3) an electrostatic discharge protection device (10; col 4 ln 59-60) comprising:

a first bipolar transistor (Q3; col 4 ln 62) and a second bipolar transistor (Q2; col 4 ln 61) coupled in series (apparent in Fig 3: series is I/O Pin-40-C-30-GND), and

an emitter (40) of the first bipolar transistor being coupled (col 5 ln 9-10) to a protected node (I/O Pin) and an emitter (30) of the second bipolar transistor being coupled (col 5 ln 8-9) to a grounded node (GND), the first bipolar transistor and the second bipolar transistor having a common collector (C; col 4 ln 62).

7. Regarding claim 2, Clukey discloses (Fig 4) the electrostatic discharge protection device of claim 1, the first bipolar transistor (Q3) and the second bipolar transistor (Q2) being npn transistors (col 5 ln 42-50, 55-58).

8. Regarding claim 7, Clukey discloses (Fig 4) the electrostatic discharge protection device of claim 2, the common collector being formed by a first n-type region (12; col 5 ln 36-37, 55-58).

9. Regarding claim 8, Clukey discloses (Fig 4) the electrostatic discharge protection device of claim 2, the first n-type region being coupled to a first p-type region (41; col 5 ln 46-47, 55-58) and a second p-type region (31; col 5 ln 46-47, 55-58), the first p-type region forming a base of the first bipolar transistor (col 5 ln 46-47, 55-58), the second p-type region forming a base of the second bipolar transistor (col 5 ln 46-47, 55-58).

10. Regarding claim 9, Clukey discloses (Fig 4) the electrostatic discharge protection device of claim 8, comprising an n-type doped isolation region (15; col 5 ln 42-43) that substantially surrounds and separates the first p-type region and the second p-type region. The term isolation region has been broadly interpreted to include any region that can separate regions from one another. Although the portions of regions 15 underlying the p-type base regions 31 and 41 serve as collector regions, the portions of

15 laterally adjacent to the p-type base regions 31 and 41 separate the p-type base regions 31 and 41.

11. Regarding claim 10, Clukey discloses (Fig 4) the electrostatic discharge protection device of claim 9, comprising a second n-type region (40; col 5 ln 49-50, 55-58) and a third n-type region (30; col 5 ln 49-50, 55-58), the second n-type region being formed within the first p-type region (40 is clearly within 41; col 5 ln 49-51) and separated from the first n-type region (40 is clearly separated from 12), the third n-type region being formed within the second p-type region (30 is clearly within 31; col 5 ln 49-51) and separated from the first n-type (30 is clearly separated from 12), the second n-type region (40) forming the emitter (col 5 ln 49; ln 10) of the first bipolar transistor (Q3) and the third n-type region (30) forming the emitter (col 5 ln 49; ln 8) of the second bipolar transistor (Q2).

12. Regarding claim 11, Clukey discloses (Fig 4) an electrostatic discharge protection device (10; col 5 ln 34) comprising:

a p-type semiconductor substrate (11; col 5 ln 34-35, 55-58);

an n-type buried layer (12; col 5 ln 36-37, 55-58) provided in the p-type semiconductor substrate (clearly 12 is in 11; col 5 ln 34-36);

a first p-type region (41; col 5 ln 46-47, 55-58) and a second p-type region (31; col 5 ln 46-47, 55-58) overlying the n-type buried layer (41 and 31 clearly overly 12), the first p-type region and the second p-type region being separated from one another (41 and 31 are clearly separated; col 5 ln 40-42);

a first n+ type region (40; col 5 ln 49-50, 55-58) provided in the first p-type region (40 is clearly in 41; col 5 ln 49-51);

a second n+ type region (30; col 5 ln 49-50, 55-58) provided in the second p-type region (30 is clearly in 31; col 5 ln 49-51); and

the first n+ type region, the first p-type region, and the n-type buried layer forming a first bipolar npn transistor (Q3; col 5 ln 9-10, 36, 46-47, 55-58), the second n+ type region , the second p-type region, and the n-type buried layer forming a second bipolar npn transistor (Q2; col 5 ln 8, 36, 45, 55-58), the first bipolar npn transistor and the second bipolar npn transistor including a common collector (12; col 5 ln 36).

Further regarding claim 11, the term n+ is a relative term, and nothing in the specification or claims prevents reading this limitation onto regions 30 and 40.

13. Regarding claim 12, Clukey discloses (Fig 4) the electrostatic discharge protection device of claim 11, the first bipolar npn transistor and the second bipolar npn transistor being coupled in series (apparent in Fig 3: series is I/O Pin-40-C-30-GND).

14. Regarding claim 13, Clukey discloses (Fig 4) the electrostatic discharge protection device of claim 12, further comprising an n-well isolation region (15; col 5 ln 42-43) that separates the first p-type region and the second p-type region. The term isolation region has been broadly interpreted to include any region that can separate regions from one another. Although the portions of regions 15 underlying the p-type base regions 31 and 41 serve as collector regions, the portions of 15 laterally adjacent to the p-type base regions 31 and 41 separate the p-type base regions 31 and 41.

15. Regarding claim 14, Clukey discloses (Fig 4) the electrostatic discharge protection device of claim 11, the first n+ type region functioning as an emitter of the first bipolar npn transistor (col 5 ln 9-10), and the second n+ type region functioning as an emitter of the second bipolar npn transistor (col 5 ln 8).

16. Regarding claim 15, Clukey discloses (Fig 4) the electrostatic discharge protection device of claim 14, the first p-type region functioning as a base region (col 5 ln 46-47) of the first bipolar npn transistor (41 is clearly part of Q3), and the second p-type region functioning as a base region (col 5 ln 46) of the second bipolar npn transistor (31 is clearly part of Q2).

17. Regarding claim 16, Clukey discloses (Fig 4) the electrostatic discharge protection device of claim 15, the n-type buried layer functioning as a common collector for both the first bipolar npn transistor and the second bipolar npn transistor (col 5 ln 36).

18. Regarding claim 18, Clukey inherently discloses a method for fabrication of an ESD protection device (Clukey discloses the structure, which, inherently, must have been formed by providing the structure), the method comprising:

providing an n-type buried layer (12; col 5 ln 36-37, 55-58) in a p-type semiconductor substrate (11; col 5 ln 34-35, 55-58);

forming a first p-type region (41; col 5 ln 46-47, 55-58) and a second p-type region (31; col 5 ln 46-47, 55-58) overlying the n-type buried layer (41 and 31 clearly overly 12), the first p-type region and the second p-type region being separated from one another (41 and 31 are clearly separated; col 5 ln 40-42);

forming a first n+ type region (40; col 5 ln 49-50, 55-58) in the first p-type region (40 is clearly in 41; col 5 ln 49-51);

forming a second n+ type region (30; col 5 ln 49-50, 55-58) in the second p-type region (30 is clearly in 31; col 5 ln 49-51); the first n+ type region, the first p-type region, and the n-type buried layer defining a first bipolar npn transistor (Q3; col 5 ln 9-10, 36, 46-47, 55-58), the second n+ type region , the second p-type region, and the n-type buried layer defining a second bipolar npn transistor (Q2; col 5 ln 8, 36, 45, 55-58).

Further regarding claim 18, the term n+ is a relative term, and nothing in the specification or claims prevents reading this limitation onto regions 30 and 40.

19. Regarding claim 19, Clukey inherently discloses (Fig 4) the method of claim 18, further comprising (Clukey discloses the structure, which, inherently, must have been formed) forming an n-well isolation region (15; col 5 ln 42-43) that separates the first p-type region and the second p-type region. The term isolation region has been broadly interpreted to include any region that can separate regions from one another. Although the portions of regions 15 underlying the p-type base regions 31 and 41 serve as collector regions, the portions of 15 laterally adjacent to the p-type base regions 31 and 41 separate the p-type base regions 31 and 41.

20. Regarding claim 20, Clukey discloses the method of claim 19, the first n+ type region functioning as an emitter of the first bipolar npn transistor (col 5 ln 9-10), and the second n+ type region functioning as an emitter of the second bipolar npn transistor (col 5 ln 8), the first p-type region functioning as a base region (col 5 ln 46-47) of the first bipolar npn transistor (41 is clearly part of Q3), the second p-type region functioning as

a base region (col 5 ln 46) of the second bipolar npn transistor (31 is clearly part of Q2), and the n-type buried layer functioning as a collector for both the first bipolar npn transistor and the second bipolar npn transistor (col 5 ln 36).

Claim Rejections - 35 USC § 103

21. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

22. Claims 3-6 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Clukey in view of Vashchenko et al. (US 6,560,081), hereinafter Vashchenko.

23. Regarding claim 3, Clukey discloses the electrostatic discharge protection device of claim 1, but does not disclose further comprising a clamp electrically coupled between the protected node and a base of the second bipolar transistor. Vashchenko is analogous art, which discloses (Fig 2) a clamp (104; col 3 ln 5-6) electrically coupled between a protected node (102; col 3 ln 1-2) and a base (116; col 3 ln 13-14, 18-19) of a bipolar transistor (114; col 3 ln 13-14).

24. Further regarding claim 3, the field of endeavor is electrostatic discharge protection devices utilizing bipolar transistors coupled between a protected node and a ground node, for both Clukey (col 4 ln 59-62; Fig 3) and Vashchenko (col 3 ln 13-15, col 4 ln 16-17, Fig 2). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Clukey by providing the clamp (104) of

Vashchenko between the protected node (Clukey I/O Pin) and the base of the bipolar transistor whose emitter is connected to ground (Clukey Q2); for at least the purpose of fast switching of the bipolar transistor (Vashchenko col 3 ln 47-49).

25. Regarding claim 4, Vashchenko discloses the clamp comprising a two-terminal circuit (110 and 112; col 3 ln 5-9).

26. Regarding claim 5, Vashchenko discloses the two-terminal circuit being configured to breakdown before the bipolar transistor (col 3 ln 41-44) to reduce the overall trigger voltage of the electrostatic discharge protection device (col 3 ln 44-47).

27. Regarding claim 6, Vashchenko discloses the two-terminal circuit comprising a diode.

28. Further regarding claim 6, the term "n-moat-p-well diode" has been neither illustrated as having a particular structure in the drawings, nor defined in the specification. Further, the specification indicates that n-moat-p-well is only one of many possible choices (page 7 ln 27-30), admitting the limitation is non-critical. The term has been broadly interpreted to mean diode.

29. Regarding claim 17, Clukey discloses the electrostatic discharge protection device of claim 16, but does not disclose further comprising a two-terminal circuit electrically coupled between the protected node and a base of the second bipolar transistor, the two-terminal circuit being configured to breakdown before the first and second bipolar transistor break down to reduce the overall trigger voltage of the electrostatic discharge protection device. Vashchenko is analogous art which discloses (Fig 2) a clamp (104; col 3 ln 5-6) electrically coupled between a protected node (102;

col 3 ln 1-2) and a base (116; col 3 ln 13-14, 18-19) of a bipolar transistor (114; col 3 ln 13-14) , the two-terminal circuit being configured to breakdown before the bipolar transistor (col 3 ln 41-44) to reduce the overall trigger voltage of the electrostatic discharge protection device (col 3 ln 44-47).

30. Further regarding claim 17, the field of endeavor is electrostatic discharge protection devices utilizing bipolar transistors coupled between a protected node and a ground node, for both Clukey (col 4 ln 59-62; Fig 3) and Vashchenko (col 3 ln 13-15, col 4 ln 16-17, Fig 2). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Clukey by providing the clamp (104) of Vashchenko between the protected node (Clukey I/O Pin) and the base of the bipolar transistor whose emitter is connected to ground (Clukey Q2); for at least the purpose of fast switching of the bipolar transistor (Vashchenko col 3 ln 47-49).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew O. Arena whose telephone number is (571) 272-5976. The examiner can normally be reached on M-F 8:30-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Loke can be reached on (571) 272-1657. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Steven Loke
Primary Examiner